Subsequently, conducting the same steps as those of the first and second embodiments enables the MOSFET M6 of the present embodiment to be manufactured.

[0099] When using such a manufacturing method, the metallic layers **60** may be parts of the source electrodes **10** and, hence, the metallic layers **50** have no need to be flattened. Therefore, a grinding step for the flattening can be omitted, thereby providing a simplified manufacturing process. Accordingly, this minimizes the occurrence of damage to the MOSFET, permitting the MOSFET to have a further increased operating quality.

[0100] While the MOSFET M**6** of the accumulation-type trench gate structure of the present embodiment has been described above with reference to a structure in which the metallic layers **50** are applied to the MOSFET M**2** of the accumulation-type trench gate structure of the second embodiment, the concept of the present invention may be applied to the structures of the MOSFETs of the first, third and fourth embodiments.

Other Embodiments

[0101] (1) While the present invention has been described above with reference to the various embodiments related to examples of the n-channel type MOSFETs in which the first electrically conductive type is of the n-type and the second electrically conductive type is of the p-type, the present invention may be applied to a MOSFET of a p-channel type with various component elements being inverted in electrically conductive types. Further, although the present invention has been described above with reference to the examples of the MOSFETs of the trench gate structure, the present invention may be applied to an IGBT (Insulated Gate Bipolar Transistor) of a similar trench structure. The IGBT can be obtained by merely altering the MOSFETs so as to convert the n-type of the electrically conductive type of the substrate **1** to the p-type in the first to fourth embodiments with other parts having the same structures as those of the MOSFETs of the first to fourth embodiments and manufactured in the same method as those of the first and fourth embodiments.

[0102] (2) Furthermore, although the present invention has been described above with reference to the first embodiment in which the trench **5** and the trenches **20**, for the p^+-type deep layers **9** to be formed, are concurrently prepared, it doesn't matter if these parts are separately formed. In this case, it doesn't matter if any of the trenches **5** and **20** is formed first. In this case, only the trenches **20** may be formed first, after which p^+-type layers **22** are formed on the trenches **20** before forming the trench **5** and subjected to CMP (Chemical Mechanical Polishing) grinding to allow only the p^+-type layers **22** to be left. This enables a process to be preferably implemented on the ground of infilling the trenches **20** with the p^+-type layers **22**.

[0103] (3) Moreover, while with the first to third embodiments, the p-type base regions **3** and the n^+-type source regions **4** are formed before the trench **5** is formed, the p-type base regions **3** and the n^+-type source regions **4** may be formed after the trench **5** is formed.

[0104] (4) While the third embodiment has been described above with reference to the MOSFET of the accumulation-type trench gate structure on which the p-type reserve layers **40** are formed, the p-type reserve layers **40** may be formed on the MOSFET of the inversion-type trench gate structure like that of the first embodiment.

[0105] (5) While the various embodiments have been described above with reference to the case wherein the p-type base regions **3** and the n^+-type source regions **4** are formed by ion-implantation, these regions may be provided by sequentially forming a p-type layer and an n-type layer on the n^--type drift layer **2**. In this case, the trenches **20** may be provided to form the p^+-type deep layers **9** after the n^+-type source regions **4** are formed. In an alternative, it may be possible to take technique of forming the p^+-type deep layers **9** by ion-implantation after the formation of the p-type base regions and subsequently forming the p^+-type contact regions **8** by ion-implantation after the formation of the n^+-type source regions **4**.

[0106] (6) While the various embodiments have been described above with reference to the case wherein the trench **5** is formed with the sidewall oriented in the [11-20] direction upon using the (000-1) c-plane, the gate oxide film **6** may be formed with a thickness greater than that of the sidewall at the bottom wall of the trench **5** even when the trench **5** is formed in the [1-100] direction with the use of a (0001) Si-plane. Even with such a structure, adopting the same structures as those of the various embodiments set forth above enables the same advantageous effects as those of the various embodiments to be obtained.

[0107] However, when using the (0001) Si-plane, an oxidizing rate is one-half of an "a"-plane. Therefore, when forming the gate oxide film **6** only by thermal oxidation, the gate oxide film **6** has the sidewall whose thickness is one-half of the thickness of the bottom wall of the trench **5**. Accordingly, the gate oxide film **6** may be prepared by thermal oxidation to allow the sidewall of the bottom wall of the trench **5** to reach a thickness of 20 nm while the remnant part of 80 nm can be prepared by a CVD (Chemical Vapor Deposition) method. In using the CVD, a film thickness, when a film is formed, is independent of a plane direction and, hence, the gate oxide film **6** has the same thickness as that of the bottom wall of the trench **5**. This allows the gate oxide film **6** to have a thickness of 90 nm, involving the film thickness caused by thermal oxidation, at the bottom wall of the trench **5**.

[0108] However, with the n^--type drift layer **2** and the p^+-type deep layers **9** of the MOSFET M**2** of the second embodiment, such a film thickness of the gate oxide film **6** causes an increase in an electric field intensity in the gate oxide film **6** at the bottom wall of the trench **5**, resulting in degraded withstand voltage. In order to obtain the same withstand voltage and electric field intensity of the MOSFET M**2** of the second embodiment, therefore, the depth of the p^+-type deep layers **9** may be preferably made to be deeper by a value of 1.5 μm and the n^--type drift layer **2** may be preferably made to have a concentration altered from a value of $8.0\times10^{15}/cm^3$ to a value of $5.0\times10^{15}/cm^3$. With such an alteration, on resistance, having a value of 1.9 $m\Omega\cdot cm^2$, increases to a value of 2.7 $m\Omega\cdot cm^2$.

[0109] Further, when indicating a crystal orientation, although a bar (-) needs to be affixed to a given numeral under normal circumstances, there is a limitation in an expression when filing a patent application based on a personal computer. Therefore, with the specification of the present patent application, the bar is affixed to the given numeral in front thereof.

[0110] While the specific embodiments of the present invention have been described above in detail, it will be appreciated by those skilled in the art that various modifications and alternatives to those details could be developed in